Abstract

With increasing demand of IoT devices, medical devices, remote sensors; the design of low power analog interface is becoming focus. Generally, for low frequency applications the Sigma Delta ADCs are used due to their very good resolution capability for such interfaces. Hence extensive work is being done to design ultra-low power Sigma Delta ADC. Most of the work has been done on optimizing loop filter design both in terms of architecture and its basic building element, op-amps. Recently, one of the prime focus of such research is Passive Sigma Delta ADC, where the loop filter is implemented with passive elements instead of active elements like op-amp.

In this work, a subthreshold region operated Passive Sigma Delta design has been explored. The thesis discusses a different analytical approach to analyze passive SDM ADC than the usual circuit level analysis used traditionally. The Simulink modeling of a passive SDM ADC was addressed to study block level performance. The circuit level implementation was carried out in Cadence environment. Both pre-and-post layout level simulations were conducted.

The passive SDM ADC designed in this work has a Sampling frequency of 10MHz, with a signal BW of 10KHz. An ENOB of 10.4 bits is achieved at power dissipation of only 4μW. The proposed ADC has very competitive FOM (Figure of Merit) in comparison with published literature.