Abstract

Experimental research on high-power converters, particularly in an academic environment, faces severe infrastructural constraints. Usually, power source and loads of required ratings are not available. Further, more importantly, the energy consumption is huge. One possibility is to establish an experimental research platform, comprising of a network of high-power converters, through which power is circulated and which draws only the losses from the mains.

This work deals with the establishment of a circulating power test set-up, comprising of two line-side PWM converters, inclusive of control and modulation methods for the two converters. Two types of circulating power test setups are developed. In the first setup, the converters are connected in parallel, on ac as well as dc sides, such that real and/or reactive power is circulated between them. In the second test setup, the dc buses of the converters are separated; hence, only reactive power circulation is possible. These setups are used to conduct heat-run tests with low energy expenditure on the PWM converters at various operating conditions up to power levels of 150 kVA. Further, these are used to validate analytically-evaluated thermal characteristics of high-power PWM converters. A safe thermal limit is derived for such converters in terms of apparent power (kVA) handled, power factor and switching frequency. The effects of voltage sag and of unequal current sharing between parallel IGBT modules on the safe thermal limit are studied.

While the power drawn by the circulating-power setup from the grid is much lower than the ratings of the individual converters, the harmonic injection into the mains by the setup could be significant since the harmonics drawn by both converters tend to add up. This thesis investigates carrier interleaving to improve the waveform quality of grid current, drawn by the circulating-power test setup. The study of carrier interleaving is quite general and covers various applications of parallel-connected converters such as unity power factor rectification, static reactive power compensation and grid-connected renewable energy systems.

In literature, carrier interleaving has been employed mainly for unity power factor rectifiers, sharing a common dc load equally. In such case, the fundamental components of the terminal voltages of the parallel converters are equal. However, when the power sharing between the two converters is unequal, or when power is circulated between the two converters, the terminal voltages of the two converters are not equal. A method to estimate rms grid current ripple, drawn

by parallel-connected converters with equal and/or unequal terminal voltages, in a synchronous reference frame is presented. Further, the influence of carrier interleaving on the rms grid current ripple is studied. The optimum interleaving angle, which minimizes the rms grid current ripple under various applications, is investigated. This angle is found to be a function of modulation index of the converters in the equal terminal voltages case. In the unequal terminal voltages case, the optimum interleaving angle is shown to be a function of the average modulation index of the two parallel converters.

The effect of carrier interleaving is experimentally studied on the reactive power circulation setup at different values of kVA and different dc bus voltages. The grid current ripple is measured for different values of interleaving angle. It is found experimentally that the optimum interleaving angle reduces the rms grid current ripple by between 37% and 48%, as compared without interleaving, at various operating conditions.

Further, the reactive power circulation test set-up is used to evaluate and compare power conversion losses corresponding to different PWM techniques such as conventional space-vector PWM (CSVPWM), bus-clamping PWM (BCPWM) and advanced bus-clamping PWM methods for static reactive power compensator (STATCOM) application at high power levels. It is demonstrated theoretically as well as experimentally that an advanced bus-clamping PWM method, termed *minimum switching loss PWM* (MSLPWM), leads to significantly lower power conversion loss than CSVPWM and BCPWM techniques at a given average switching frequency.