Abstract

Neutral-point-clamped (NPC) three-level inverter is capable of handling higher dc bus voltage and producing output waveform of better quality than a conventional two-level inverter. The main objective of the present work is to analyze the existing PWM schemes for two-level and three-level inverters in terms of line current ripple, and to design new PWM techniques for the NPC inverter to reduce line current distortion.

Various discontinuous PWM or bus-clamping PWM (BCPWM) methods for a two-level voltage source inverter are analyzed in terms of rms line current ripple, which is evaluated by integrating the error voltage (i.e. error between the applied and reference voltages). The BCPWM schemes can be broadly classified into continual-clamp PWM (CCPWM) and split-clamp PWM (SCPWM). It is shown that split-clamp PWM scheme leads to lower harmonic distortion than CCPWM scheme. Further, advanced bus-clamping PWM (ABCPWM) methods for a two-level inverter are also studied. These methods clamp each phase to the positive and negative DC terminals over certain intervals as in BCPWM schemes, and also switch each phase at double the nominal frequency in certain other intervals unlike in BCPWM. Analytical closed-form expressions are derived for the total rms harmonic distortion due to SCPWM, CCPWM and ABCPWM schemes.

Existing sinusoidal and bus-clamping PWM schemes for three-level NPC inverters are also analyzed in the space vector domain. These methods are compared in terms of line current ripple analytically as well as experimentally. As earlier, closed-form expressions are derived for the harmonic distortion factors corresponding to centered space vector PWM (CSVPWM) and the various BCPWM methods.

A three-level inverter can be viewed as an equivalent two-level inverter in each sixth of the fundamental cycle or hextant. This is widely used to simplify the control of an NPC inverter. Further, this approach makes it simple to extend the BCPWM and ABCPWM methods for two-level inverters to three-level inverters. Furthermore, the

method of analysis of line current ripple for the two-level inverter can also be easily extended to the three-level case.

The pivot vector, which is half the length of the longest voltage vectors produced by the NPC inverter, acts as an equivalent null vector for the conceptual two-level inverter. Each pivot vector can be produced by two inverter states termed as “pivot states”. Typically, in continuous modulation methods for NPC inverter such as sinusoidal PWM and centered space vector PWM, the switching sequence (i.e. the sequence in which the voltage vectors are applied) begins and ends with the same pivot vector in each subcycle, which is equivalent to a half-carrier cycle. To be more precise, the switching sequence starts with one pivot state and ends with the other in each subcycle.

However, in case of BCPWM schemes, only one pivot state is used in a subcycle. The choice of pivot state results in a variety of BCPWM schemes for an NPC inverter. Different BCPWM schemes are evaluated in terms of rms line current ripple. The optimal BCPWM, which minimizes the rms current ripple, is determined for an NPC inverter, controlled as an equivalent two-level inverter.

Further, four new switching sequences are proposed here for a three-level inverter, controlled as a conceptual two-level inverter. These sequences apply the pivot vector only once, but employ one of the other two vectors twice within the subcycle. These four switching sequences are termed as “ABCPWM sequences” for three-level inverter. These sequences exploit the flexibility available in the space vector approach to PWM to switch a phase more than once in a subcycle, which results in the application of an active vector twice within the subcycle.

Influence of the proposed ABCPWM sequences on the line current ripple over a subcycle is studied. The various sequences are compared in terms of rms line current ripple over a subcycle. An analytical closed-form expression for rms line current ripple over a subcycle is derived in terms of reference magnitude, angle of reference voltage vector, and subcycle duration for each of the sequences. Further, closed-form expressions are also derived for the rms current ripple over a line cycle in terms of modulation index and subcycle duration, corresponding to the various sequences.

The four proposed ABCPWM sequences for the NPC inverter can be grouped into two pairs of sequences. Each pair of sequences is shown to perform better than the

individual sequences, if the two sequences are employed in appropriate spatial regions. Hence, with these two pairs of sequences, two hybrid PWM schemes are proposed. Finally, a hybrid PWM technique is proposed which employs all five sequences (conventional and proposed four sequences) in spatial regions where each performs the best. This is termed as “five-zone hybrid PWM”. The total harmonic distortion (THD) in the motor current, pertaining to all the proposed schemes, is studied theoretically over the entire range of linear modulation.

The theoretical investigations are validated experimentally on a 2.2 kW, 415V, 4.9A, 50 Hz induction motor drive. The no-load current THD is measured over a range of fundamental frequency from 10 Hz to 50 Hz in steps of 2 Hz for the various PWM methods. Theoretical and experimental results bring out the reduction in current THD due to the proposed BCPWM schemes at fundamental frequencies of 45 Hz and above, compared to CSVPWM. The ABCPWM methods improve the performance at higher as well as lower modulation indices. Further improvement is achieved with the proposed five-zone hybrid PWM. At the rated frequency (50 Hz) of the drive, the improvement in line current distortion is around 36% with this hybrid PWM scheme over CSVPWM. The reduction in THD is also experimentally verified at different loads on the motor.

The difference between the top and bottom capacitor voltages is measured at various operating conditions, corresponding to CSVPWM and the proposed schemes. No significant difference is observed in the dc neutral voltage shifts with the different proposed schemes and CSVPWM method. Thus, the proposed methods improve the THD at low and high speed ranges without appreciable worsening of the dc voltage unbalance.