# Abstract

Power dissipated during scan testing is becoming increasingly important for today's very complex sequential circuits. It is shown that the power dissipated during test mode operation is in general higher than the power dissipated during functional mode operation, the test mode average power may sometimes go upto 3x and the peak power may sometimes go upto 30x of normal mode operation. The power dissipated during the scan operation is primarily due to the switching activity that arises in scan cells during the shift and capture operation. The switching in scan cells propagates to the combinational block of the circuit during scan operation, which in turn creates many transition in the circuit and hence it causes higher dynamic power dissipation. The excessive average power dissipated during scan operation causes circuit damage due to higher temperature and the excessive peak power causes yield loss due to IR-drop and cross talk. The higher peak power also causes the thermal related issue if it last for sufficiently large number of cycles. Hence, to avoid all these issues it is very important to reduce the peak power during scan testing. Further, in case of multi-module SoC testing the reduction in peak power facilitates in reducing the test application time by scheduling many test sessions parallelly. In this dissertation we have addressed all the above stated issues. We have proposed three different techniques to deal with the excessive peak power dissipation problem during test.

The first solution proposes an efficient graph theoretic methodology for test vector reordering to achieve minimum peak power supported by the given test vector set. Three graph theoretic problems are formulated and corresponding algorithms to solve the problems are proposed. The proposed methodology also minimizes average power for

the given minimum peak power. Further, a lower bound on minimum achievable peak power for a given test set is defined. The results on several benchmarks show that the proposed methodology is able to reduce peak power significantly.

To address the peak power problem during scan test-cycle (the cycle between launch and capture pulse) we have proposed a scan chain reordering technique. A new formulation for scan chain reordering as TSP (Traveling Sales Person) problem and a solution is proposed. The experimental results show that the proposed methodology is able to minimize considerable amount of peak power compared to the earlier proposals.

The capture power (power dissipated during capture cycle) problem in testing multi chip module (MCM) is also addressed. We have proposed a methodology to schedule the test set to reduce capture power. The scheduling algorithm consist of reordering of test vector and insertion of idle cycle to prevent capture cycle coincidence of scheduled cores. The experimental results show the significant reduction in capture power without increase in test application time.