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Title of the thesis: **A New Class of Single DC-link Fed Multilevel Inverter Topologies for Grid Connected Photovoltaic Systems with Reduced Component Count and Inherent Capacitor Balancing**

ABSTRACT

Grid integration of photovoltaic (PV) energy sources has been mostly governed by conventional two-level voltage source inverters. These topologies have significant switching power losses, dV/dt stress and THD level at lower switching frequencies. The above issues can be solved by introducing more voltage levels through multilevel converters. Conventional multilevel converters have many issues like neutral point voltage drift in neutral point clamped (NPC) topology, floating capacitor charge balance in flying capacitor (FC) topology and large number of isolated DC sources in cascaded half bridge (CHB) topology when scaling them for higher number of voltage levels. Additionally, active power devices and its associated gate drivers, clamping diodes, flying capacitors and DC link capacitors also increase with levels. Hence, it is desirable to generate a multilevel voltage output with a single DC link and with the reduced components count. This thesis proposes a new way of generating multilevel voltage output using a single DC source and with the least components count. The thesis also proposes a new gate driver that can be operated at wide duty cycle ratios and wide band frequency.

The thesis presents five major contributions as follows,

1. 16 switch five level inverter for isolated grid tied systems
2. 12 switch five level inverter for isolated grid tied systems
3. Inherent DC link capacitor balancing
4. Extension of five level inverter topologies to higher levels
5. A Wide duty cycle range wide band high frequency isolated gate driver for multilevel power converters

First part of the research work, presents a novel five level inverter for high power isolated grid connection, which is powered by a single DC source. The proposed topology employs overall 16 active power devices, two DC link capacitors and a Scott-T transformer. Out of 16 power switches, 8 switches operate at high frequency and remaining 8 operate at the fundamental frequency. The DC link capacitors have an inherent voltage balancing which eliminates the requirement of charge balancing circuit or complex control algorithm. Additionally, necessity of expensive voltage sensors are also mitigated. The five level converter initially generate five level voltages in two phase system, and then they are transformed to three phases by using a Scott-T transformer. Operation of the proposed five level inverter (1 kW) is tested experimentally by connecting it to a three phase grid with unity power factor control. Second part follows the footsteps of the first topology.

The second topology presents a grid connected five level inverter with only 12 power devices. This topology is also powered by a single DC source. Eight (8) out of 12 power devices are switched at fundamental frequency (variable) and the remaining devices are switched at high frequency. The proposed inverter is validated experimentally by connecting it to a three phase grid. The performance of capacitor voltage balancing under steady state and transient loading conditions is verified.

Third part of the thesis discusses about the inherent charge balancing phenomenon of the DC link capacitors for the proposed inverter topologies. In both the topologies, the DC link capacitors have inherent voltage balancing capability. This feature eliminates the requirement of voltage sensors and complex control schemes which are generally employed in the conventional multilevel inverters.

In fourth part of the research work, a wide band frequency and wide duty cycle operated isolated gate driver with only a single auxiliary power supply is proposed. The proposed gate driver is specifically advantageous for multilevel inverters as all the gate drivers can be powered by a single auxiliary power supply. The integrated gate driver has features like, wide duty cycle (0 - 100%) and wide band frequency (ranging from DC to 1 MHz) operation, short circuit/over current, and miller clamp protections. The performance of the gate driver is validated experimentally followed by a LTSPICE software simulations.

Finally, a generalized multilevel inverter topology based on the proposed five level inverter topologies with only a single DC source is presented. Multilevel output is obtained by cascading H-bridge modules on either side of the five level converter after the unfolding stage. Connecting 'n' number of H-bridge modules per phase to the five level converter leads to $[8n+1]$ levels of the output voltage. Feasibility of the converter is validated by testing a nine level inverter configuration. The proposed concept uses least active power devices, DC link capacitor, flying capacitor, and diodes compared to the existing single DC link fed multilevel inverter topologies.

All the above presented topologies and circuits are extensively tested in simulation and in the experimentation in laboratory for three phase grid connected unity power factor operation. A 1 kW, 50 Hz fundamental and 10 kHz switching inverters was developed for the experimental studies. The inverter is used for the grid integration of DC sources with 192 V, 1 kW power rating. The inverter prototype consists of power semiconductor switches of rating 1200 V and 75 A insulated gate bipolar transistor (IGBT) half bridge Semikron modules (SKM75GB12T4). The proposed gate drivers were used to drive the power IGBTs. The Scott-T transformer is realized using two single phase transformers with an appropriate winding turns ratio. The current control and PWM signal generation is carried in a digital signal processor (DSP-TMS320F28335) with a clock frequency of 150 MHz. The grid voltage and currents were sensed by using LEM make voltage (LV-25P) and current (LA-55P) sensors. The sensed voltage and current data is fed to the analog to digital converter (ADC) which internally exists in the DSP. All the computations and frame transformations were also carried within the DSP. The dead time for the IGBT modules is generated as $1\mu\text{s}$. The testing was done by connecting the proposed inverters to the grid. The inverter performance is validated at various loading conditions. The inherent capacitor balancing was also validated under steady state and transient loading conditions.

The proposed inverter topologies exhibits advantages like, reduced components count, single DC link operation, inherent capacitor voltage balancing, fundamental switching devices and inherent isolation. Overall size of the proposed inverters is less compared to the conventional five level inverters for grid connected applications where isolation is mandatory. The inherent capacitor voltage balancing also eliminates the requirement of expensive voltage sensors, complex control circuits and algorithms. The fewer active components count results in simple control architecture and improves reliability of the inverters to a large extent. The experimental validation shows that the proposed inverter topologies can be considered as viable solutions for the high power isolated grid tied photovoltaic systems.
